wherein said some of the impurity regions are located between the plurality of channel regions in the semiconductor film.

2. (Amended) A device according to claim 1, wherein at least two of said impurity regions overlapped with the gate electrode contain an element at a concentration of 2 x $10^{16}$ to 5 x $10^{19}$ atoms/cm$^3$, and at least one of the impurity regions overlapped with the gate electrode contain the element at a concentration of 5 x $10^{19}$ to 3 x $10^{21}$ atoms/cm$^3$.

3. (Amended) A device according to claim 1, wherein a thickness of a gate insulating film of a TFT in said driver circuit portion is thinner than that of the gate insulating film of a TFT in the pixel portion.

4. (Amended) A device according to claim 1, wherein a gate insulating film of a TFT in said driver circuit portion and a dielectric of a storage capacitor formed in said pixel portion comprise the same material and have the same film thickness.

6. (Amended) A display device comprising a pixel portion and a driver circuit portion on a substrate, said pixel portion comprising:

a semiconductor film comprising a plurality of channel forming regions, a plurality of low concentration impurity regions, a high concentration impurity region, a source region, and a drain region; and

a gate electrode overlapping with the channel forming regions, some of the low concentration impurity regions, and the high concentration impurity region, with a gate insulating film interposed therebetween,

wherein said some of the low concentration impurity regions and the high concentration impurity region are located between the plurality of the channel regions in the semiconductor film.

7. (Amended) A device according to claim 6, wherein each of said low concentration impurity regions contains an element at a concentration of $2 \times 10^{16}$ to $5 \times 10^{19}$ atoms/cm$^3$, and said high concentration impurity region contains the element at a concentration of $5 \times 10^{19}$ to $3 \times 10^{21}$ atoms/cm$^3$.

8. (Amended) A device according to claim 6, wherein a thickness of a gate insulating film of a TFT in said driver circuit portion is thinner than that of the gate insulating film of a TFT in said pixel portion.

9. (Amended) A device according to claim 6, wherein a gate insulating film of a TFT in said driver circuit portion and a dielectric of a storage capacitor formed in said pixel portion comprise the same material and have the same film thickness.

15. (Amended) A display device comprising a pixel portion and a driver circuit portion on a substrate, said pixel portion comprising:

a semiconductor film comprising at least two channel forming regions, at least one first impurity region, at least one second impurity region, a source region, and a drain region; and

a gate electrode overlapped with said two channel forming regions and the first impurity region, and a part of the second impurity region with a gate insulating film interposed therebetween,

wherein one of the channel forming regions is located between the first impurity region and the second impurity region.

16. (Amended) A device according to claim 15, wherein a thickness of a gate insulating film of a thin film transistor in said driver circuit portion is thinner than that of the gate insulating film in the pixel portion.

18. (Amended) A display device comprising a pixel portion and a driver circuit portion on a substrate, said pixel portion comprising:

a semiconductor film having at least two channel forming regions, first and second low concentration impurity regions, high concentration impurity regions, a source region, and a drain region; and

a gate electrode overlapping with said two channel forming regions, the first low concentration impurity regions, the high concentration impurity region, and portions of the second impurity regions, with a gate insulating film interposed therebetween,

wherein the high concentration impurity region is located between the channel forming regions.

19. (Amended) A device according to claim 18, wherein a thickness of a gate insulating film of a thin film transistor in said driver circuit portion is thinner than that of the gate insulating film in the pixel portion.

Please add new claims 21-42 as follows:

--21. A device according to claim 1, wherein the impurity regions have the same conductivity as the source and drain regions.

22. A device according to claim 2, wherein the element belongs to group XV in the periodic table.

23. A device according to claim 6, wherein the low and high concentration impurity regions have the same conductivity as the source and drain regions.

24. A device according to claim 6, wherein the high concentration impurity region are located between a pair of the low concentration impurity regions under the gate electrode.

25. A device according to claim 7, wherein the element belongs to group XV in the periodic table.

26. A device according to claim 15, wherein the first and second impurity regions have the same conductivity as the source and drain regions.

27. A device according to claim 15, wherein each of the first and second impurity region contains an at a concentration of $2 \times 10^{16}$ to $5 \times 10^{19}$ atoms/cm$^3$, and

wherein the semiconductor film further comprises a third impurity region including the element at a concentration of $5 \times 10^{19}$ to $3 \times 10^{21}$ atoms/cm$^3$.

28. A device according to claim 27, wherein the element belongs to group XV in the periodic table.

29. A device according to claim 15, wherein a gate insulating film of a TFT in said driver circuit portion and a dielectric of a storage capacitor formed in said pixel portion comprise the same material and have the same film thickness.

30. A device according to claim 18, wherein the first and second low concentration impurity regions and the high concentration impurity region have the same conductivity as the source and drain regions.

31. A device according to claim 18, wherein the high concentration impurity region is located between a pair of the first low concentration impurity regions.

32. A device according to claim 18, wherein each of the first and second concentration impurity region contains an at a concentration of $2 \times 10^{16}$ to $5 \times 10^{19}$ atoms/cm$^3$, and the high concentration impurity region includes the element at a concentration of $5 \times 10^{19}$ to $3 \times 10^{21}$ atoms/cm$^3$.

33. A device according to claim 32, wherein the element belongs to group XV in the periodic table.

34. A device according to claim 18, wherein a gate insulating film of a TFT in said driver circuit portion and a dielectric of a storage capacitor formed in said pixel portion comprise the same material and have the same film thickness.

35. A semiconductor device comprising:

a semiconductor film having at least first and second channel forming regions, first, second, third, and fourth low concentration impurity regions, a high concentration impurity regions, a source region, and a drain region; and

a gate electrode overlapping with the first and second channel forming regions, the second and third low concentration impurity regions, the high concentration impurity region, and portions of the first and fourth low concentration impurity regions, with a gate insulating film interposed therebetween,

wherein the high concentration impurity region is located between the first and second channel forming regions.

36. A device according to claim 35, wherein the low concentration impurity regions and the high concentration impurity region have the same conductivity as the source and drain regions.

37. A device according to claim 35, wherein the high concentration impurity region is located between the second and third low concentration impurity regions in the semiconductor film.

38. A device according to claim 35, wherein each of said low concentration impurity region contains an element at a concentration of $2 \times 10^{16}$ to $5 \times 10^{19}$ atoms/cm$^3$, and said high concentration impurity region contains the element at a concentration of $5 \times 10^{19}$ to $3 \times 10^{21}$ atoms/cm$^3$

39. A device according to claim 38, wherein the element belongs to group XV in the periodic table.

40. A device according to claim 35, wherein a thickness of a gate insulating film of a thin film transistor in said driver circuit portion is thinner than that of the gate insulating film in the pixel portion.

41. A device according to claim 35, wherein a gate insulating film of a TFT in said driver circuit portion and a dielectric of a storage capacitor formed in said pixel portion comprise the same material and have the same film thickness.

42. An electronic equipment comprising a semiconductor device according to claim 35, wherein said electronic equipment is selected from the group consisting of a video camera, a digital camera, a projector, a projection TV, a goggle type displays, a navigation system, a sound reproduction device, a notebook type personal computer, a game machine, a portable information terminal, a mobile computer, a portable telephone, a portable game machine, an electronic books, and an image reproduction devices having recording medium.--

## REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the present application.

The Examiner's non-final Office Action dated May 2, 2001 has been received and its contents carefully noted.

Claims 1-10 and 15-20 were pending in this application, of which claims 1, 6, 15 and 18 are independent. Claims 1-4, 6-9, 15, 16, 18 and 19 have been amended and new claims 21-42 have been added, of which claim 35 is independent. Accordingly, 1-10 and 15-42 are pending in this application and are believed to be in condition for allowance.

### *Claims 1, 2, 5-7, 10, 15, 17, 18 and 20 are Patentable Over Yudasaka and Kobayashi Under 35 U.S.C. § 103(a)*

Claims 1, 2, 5-7, 10, 15, 17, 18 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yudasaka et al., U.S. Patent No. 5,953,582 (Yudasaka) in view of Kobayashi et al., U.S. Patent No. 5,767,930 (Kobayashi).